CLAIMS:

1. A network device comprising:

a buffer memory having a plurality of memory locations including redundant memory locations, said memory locations having addresses;

a plurality of network ports;

a memory controller coupled to said buffer memory and configured to read and write data from and to said buffer memory;

a first plurality of fuses coupled to said redundant memory locations of said buffer memory;

a second plurality of fuses coupled to said memory controller and configured to store an address of a failed memory location of said plurality of memory locations; and

a built-in self test unit coupled to said buffer memory and to said second plurality of fuses, and configured to perform a test of said buffer memory to determine an address of a failed memory location of said plurality of memory locations, and to store said address of said failed memory location in a fuse of said second plurality of fuses; and

wherein said memory controller is configured to prevent a use of said failed memory location based on said address stored in said fuse.

2. The network device of claim 1, wherein said built-in self test unit is configured to determine an address of a second failed memory location of said plurality of memory locations and to store said address of said second failed memory location in a fuse of said fist plurality of fuses associated with a redundant memory location of said

plurality of memory locations, and said memory controller is configured to use said redundant memory location instead of said second failed memory location.

3. The network device of claim 1, further comprising:

a location determining unit coupled to said built-in self test unit and configured to determine the address of failed memory locations.

4. The network device of claim 3, wherein said built-in self test unit is configured to generate address information related to failed memory locations and output said address information to said location determining unit, and said location determining unit is configured to determine which fuses to blow based on said address information.

5. The network device of claim 1, further comprising:

a fuse blowing unit coupled to said built-in self test unit and configured to blow a fuse of said first plurality of fuses in order to enable said fuse and store an address in said fuse.

6. The network device of claim 1, further comprising:

a flow controller coupled to said plurality of network ports and to said memory controller, and configured to request buffer pointers based on a data packet received at a network ports of said plurality of network ports;

wherein, said memory controller is configured to provide buffer pointers to said flow controller without using any failed memory locations based on data stored in said second plurality of fuses.

7. The network device of claim 1, wherein each fuse of said second plurality of fuses include a bit for identifying if said fuse is enabled and a plurality of bits for storing an address of a failed memory location.

8. The network device of claim 1, wherein said buffer memory comprises embedded memory and said built-in self test unit is configured to perform a wafer test.

9. The network device of claim 8, wherein said buffer memory comprises 0.13 μm to 0.18μm SRAM.

10. The network device of claim 3, wherein said location determining unit comprises an external processing unit.

11. The network device of claim 5, wherein said fuse blowing unit comprises an external fuse blowing device.

12. The network device of claim 2, wherein said device is configured to utilize all of said first plurality of fuse means before using said second plurality of fuse means.

13. A method for testing buffer memory, said method comprising the steps of:

testing a buffer memory having a plurality of memory locations including redundant memory locations, to determine if any of said plurality of memory locations are unusable;

determining an address of a first unusable memory location of said plurality of memory locations;

storing the address of said first unusable memory location; and

preventing a use of said first unusable memory location based on the stored address of said unusable memory location.

14. The method of claim 13, further comprising steps of:

providing a first plurality of fuses associated with said redundant memory locations;

determining an address of a second unusable memory location of said plurality of memory locations;

storing the address of said second unusable memory location in a fuse of said first plurality of fuses associated with a redundant memory location of said plurality of memory locations; and

allowing a use of said redundant memory location instead of said second failed memory location based on said fuse.

15. The method of claim 13, further comprising step of:

providing a network device having a buffer memory;

wherein said step of testing the buffer memory comprises performing a built-in test, said network device automatically performing said step for testing the buffer memory at start-up.

16. The method claim 13, further comprising a step of:

providing an address determining unit for determining addresses of unusable memory locations.

17. The method of claim 13, further comprising steps of:

determining a total number of failed memory locations;

restricting a number of buffer pointers to a number equal to a total number of memory locations minus a total number of failed memory locations.

18. The method of claim 13, wherein said storing step comprises storing said address in a fuse, said fuse including a bit for identifying if said fuse is enabled and a plurality of bits for storing an address of a failed memory location, and setting said bit for identifying if said fuse is enabled and storing said address in said plurality of bits.

19. The method of claim 13, wherein said step of testing the buffer memory comprises testing embedded memory and said testing step comprises performing a wafer test.

20. A network device comprising:

a buffer memory means having a plurality of memory locations including redundant memory locations, said memory locations having addresses;

a plurality of network ports;

a memory controller means coupled to said buffer memory and for reading and writing data from and to said buffer memory means;

a first plurality of fuse means coupled to said redundant memory locations of said buffer memory means;

a second plurality of fuse means coupled to said memory controller and for storing an address of a failed memory location of said plurality of memory locations; and

a built-in self test means coupled to said buffer memory means and to said second plurality of fuse means, for performing a test of said buffer memory means to determine an address of a failed memory location of said plurality of memory locations, and for storing said address of said failed memory location in a fuse means of said second plurality of fuse means; and

wherein said memory controller means is for preventing a use of said failed memory location based on said address stored in said fuse means.

21. The network device of claim 20, wherein said built-in self test means is configured to determine an address of a second failed memory location of said plurality of memory locations and store said address of said failed memory location in a fuse means of said first plurality of fuse means associated with a redundant memory location of said plurality of memory locations, and said memory controller means is configured to use said redundant memory location instead of said second failed memory location.

22. The network device of claim 20, further comprising:

a location determining means coupled to said built-in self test means and for determining the address of failed memory locations.

23. The network device of claim 22, wherein said built-in self test means generates address information related to failed memory locations and outputs said address information to said location determining means, and said location determining means determining which fuses to blow based on said address information.

24. The network device of claim 20, further comprising:

a fuse blowing means coupled to said built-in self test means, for blowing a fuse means of said first plurality of fuse means in order to enable said fuse means and store an address in said fuse means.

25. The network device of claim 20, further comprising:

a flow controller means coupled to said plurality of network ports and to said memory controller means, for requesting buffer pointer means based on a data packet received at a network ports of said plurality of network ports;

wherein said memory controller means is configured to provide buffer pointer means to said flow controller means without using any failed memory locations based on data stored in said second plurality of fuse means.

26. The network device of claim 20, wherein each fuse means of said second plurality of fuse means include a bit for identifying if said fuse means is enabled and a plurality of bits for storing an address of a failed memory location.

27. The network device of claim 20, wherein said buffer memory means comprises embedded memory means and said built-in self test means comprises a wafer test means.

28. The network device of claim 27, wherein said buffer memory means comprises 0.13 μm to 0.18μm SRAM.

29. The network device of claim 22, wherein said location determining means comprises an external processing unit.

30. The network device of claim 24, wherein said fuse blowing means comprises an external fuse blowing device.

31. The network device of claim 22, wherein said device is configured to utilize all of said first plurality of fuse means before using said second plurality of fuse means.